IN THE CLAIMS

Claim 1 (currently amended): A method of forming a CMOS semiconductor ~~materials~~ device with a PFET area and an NFET area formed on a semiconductor substrate, said PFET area being covered with a PFET gate dielectric layer and said NFET area covered with an NFET gate dielectric layer composed of silicon oxide with different degrees of nitridation thereof,

providing a silicon substrate with a PFET area and an NFET area,

forming a PFET gate oxide layers over said PFET area and an NFET gate oxide layer over said NFET area,

providing nitridation of said PFET gate oxide layer above said PFET area to form said PFET gate dielectric layer above said PFET area with a first optimized concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area,

providing nitridation of said NFET gate oxide layer to form said NFET gate dielectric layer above said NFET area with a second optimized concentration level of nitrogen atoms in said NFET gate dielectric layer above said NFET area,

whereby an NFET concentration level of nitrogen atoms in said NFET gate dielectric layer is different from a PFET concentration level of nitrogen atoms in said PFET gate dielectric layer.

Claim 2 (original): The method of claim 1 including performing the following steps with one thereof preceding the other:

forming an NFET mask over said NFET area prior to beginning nitridation of said PFET gate oxide layer, then performing PFET gate dielectric nitridation thereof, and immediately thereafter removing said NFET mask, and

forming a PFET mask over said PFET area prior to beginning nitridation of said NFET gate oxide layer, then performing NFET gate dielectric nitridation thereof, and immediately thereafter removing said PFET mask.

Claim 3 (currently amended): The method of claim 1 including performing the following steps with one thereof preceding the other:

forming a single mask over one of said NFET area and said PFET area prior to beginning nitridation leaving the other <u>one</u> of said ~~regions~~ <u>NFET area and said PFET area</u> as an unmasked <u>area</u> ~~region~~, performing gate dielectric nitridation of said unmasked <u>area</u> ~~region~~, and immediately thereafter removing said single mask, and

performing gate dielectric nitridation into both said NFET area and said PFET area adding an [[equal]] <u>additional</u> concentration of nitrogen to said NFET gate oxide layer and said PFET gate oxide layer.

Please cancel claim 4.

Claim 4 (canceled)

Claim 5 (original): The method of claim 1 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

Claim 6 (original): The method of claim 2 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

Claim 7 (original): The method of claim 3 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

Claim 8 (original): The method of claim 4 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

Claim 9 (currently amended): A method of forming a CMOS semiconductor ~~materials~~ device with a PFET area and an NFET area formed on a semiconductor substrate, said PFET area being covered with a PFET gate dielectric layer and said NFET area covered with an NFET gate dielectric layer composed of silicon oxide and different degrees of nitridation thereof,

providing a silicon substrate with a PFET area and an NFET area,

forming a PFET gate oxide layer over said PFET area and an NFET gate oxide layer over said NFET area,

forming an NFET mask over said NFET area prior to beginning nitridation of said PFET gate oxide layer, then performing PFET gate dielectric nitridation ~~providing nitridation~~ of said PFET gate oxide layer above said PFET area to form said PFET gate dielectric layer above said PFET area with a first optimized concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area and then removing said NFET mask,

forming a PFET mask over said PFET area prior to beginning nitridation of said NFET gate oxide layer, then performing NFET gate dielectric nitridation ~~providing nitridation~~ of said NFET gate oxide layer to form said NFET gate dielectric layer above said NFET area producing a second optimized concentration level of nitrogen atoms in said NFET gate dielectric layer above said NFET area, and then removing said PFET mask, whereby an NFET concentration level of nitrogen atoms in said NFET gate dielectric layer is less than said first concentration level of nitrogen atoms in said PFET gate dielectric layer, and

said NFET gate dielectric layer and said PFET gate dielectric layer have substantially the same thickness.

Claim 10 (currently amended): The method of claim 9 including performing the following steps with one thereof preceding the other:

~~forming an NFET mask over said NFET area prior to beginning nitridation of said PFET gate oxide layer, then performing PFET gate dielectric nitridation thereof, and immediately thereafter removing said NFET mask, and~~

~~forming a PFET mask over said PFET area prior to beginning nitridation of said NFET gate oxide layer, then performing NFET gate dielectric nitridation thereof, and immediately thereafter removing said PFET mask,~~

forming a single mask over one of said NFET area and said PFET area prior to beginning nitridation leaving the other <u>one</u> of said ~~regions~~ <u>NFET area and said PFET area</u> as an unmasked ~~region~~ <u>area</u>, performing gate dielectric nitridation of said unmasked <u>area</u> ~~region~~, and immediately thereafter removing said single mask, and

performing gate dielectric nitridation into both said NFET area and said PFET area adding an [[equal]] <u>additional</u> concentration of nitrogen to said NFET gate oxide layer and said PFET gate oxide layer, with a resulting total nitrogen content higher in said PFET gate oxide layer.

Please cancel claim 11

Claim 11 (canceled)

Claim 12 (original): The method of claim 9 including providing grater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

Claim 13 (original): The method of claim 1 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

Claim 14 (original): The method of claim 2 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

Claim 15 (original): The method of claim 3 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

Claim 16 (original): The method of claim 4 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

Claim 17 (original): The method of claim 5 wherein the nitridation process is performed at a temperature below the melting maximum temperature that the masking material can withstand.

Claim 18 (original): The method of claim 6 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

Claim 19 (original): The method of claim 7 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

Claim 20 (currently amended): A CMOS semiconductor device with a PFET area and an NFET area formed on a semiconductor substrate, said PFET area being covered with a PFET gate dielectric layer and said NFET area covered with an NFET gate dielectric layer composed of silicon oxide and different degrees of nitridation thereof comprising:

a silicon substrate with said PFET area and said NFET area,

a PFET gate dielectric layer over said PFET area and an NFET gate dielectric layer over said NFET area,

said PFET gate dielectric layer above said PFET area being nitrided with a first optimized concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area,

said NFET gate dielectric layer above said NFET area being nitrided with a second optimized concentration level of nitrogen atoms in said NFET gate dielectric layer above said NFET area,

said PFET gate dielectric layer and said NFET gate dielectric layer having different optimized levels of nitridation whereby a PFET concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area is different from [[the]] an NFET concentration level of nitrogen atoms in said NFET gate dielectric layer.

Please add the following claims:

Claim 21 (new): The method of claim 1 including performing the following steps:

first forming a base oxide mask over a base oxide layer for a capacitor area in said substrate,

then performing nitridation of a said gate dielectric layer followed by forming a mask thereover after removing said base oxide mask over said capacitor area, and

then performing nitridation of said base oxide layer above said capacitor area thereby converting said base oxide layer into a capacitor dielectric layer.

Claim 22 (new): The method of claim 9 including performing the following steps:

first forming a base oxide mask over a base oxide layer for a capacitor area in said substrate,

then performing nitridation of a said gate dielectric layer followed by forming a mask thereover after removing said base oxide mask over said capacitor area, and

then performing nitridation of said base oxide layer above said capacitor area thereby converting said base oxide layer into a capacitor dielectric layer.